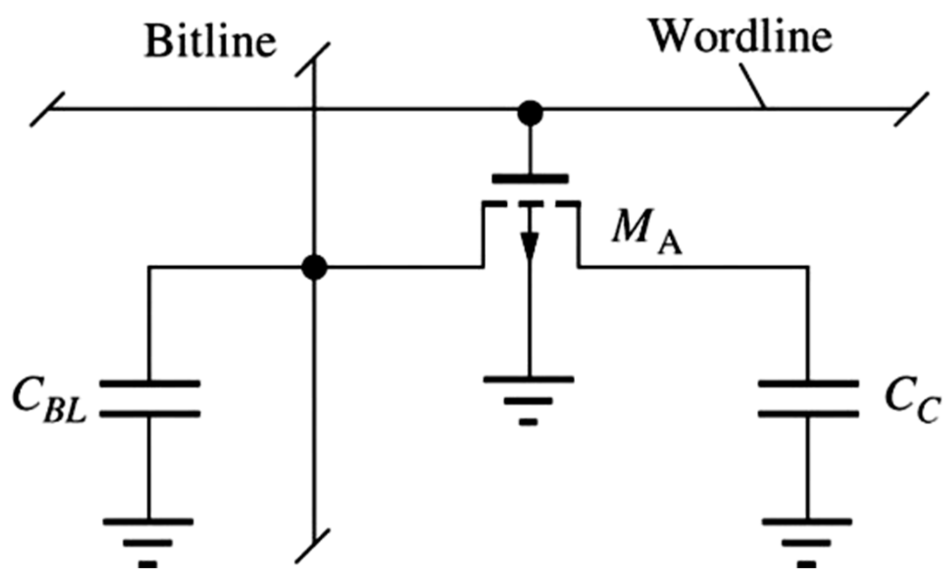
Announcements

- Homework #9 due Friday.
- Addition to Final Project:

  Evaluation (10 points)
  Evaluate and compare your two designs regarding performance, reliability, cost, and power dissipation. Discuss the extent to which these factors could be improved or traded-off in a final product.
- Schedule Final Project demo with TAs for this Thursday and Friday.

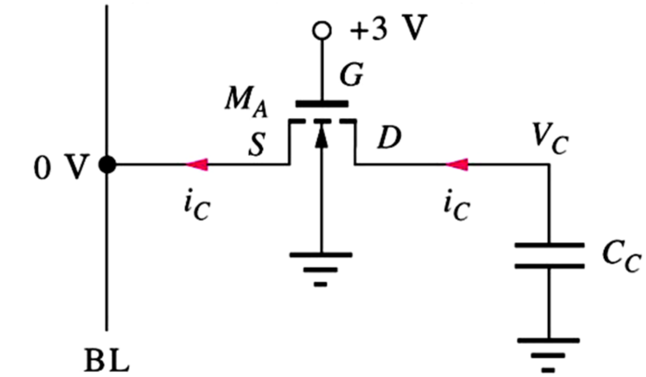
Dynamic Memory Cells
The One-Transistor (1-T) Cell

- The 1-T cell uses a capacitor for its storage element (data is represented as either a presence or absence of a charge)
- Due to leakage currents in M_A, the data will eventually be corrupted, hence it needs to be refreshed



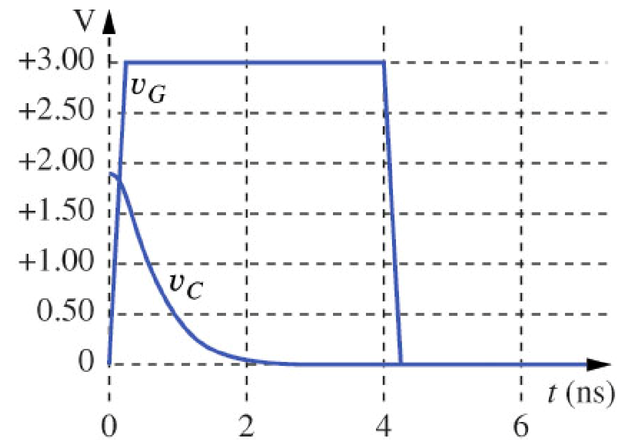
The 1-T Cell

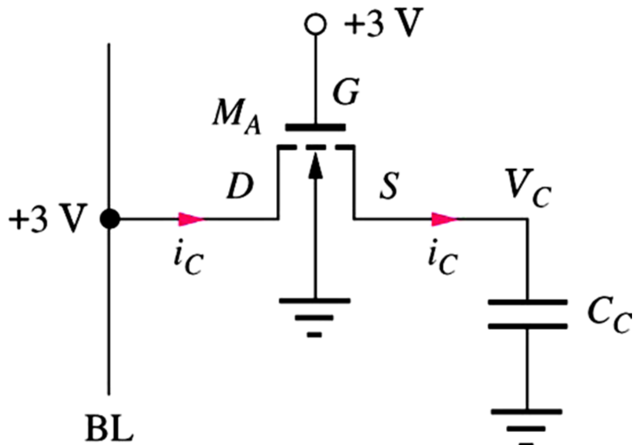
Data Storage



(a)

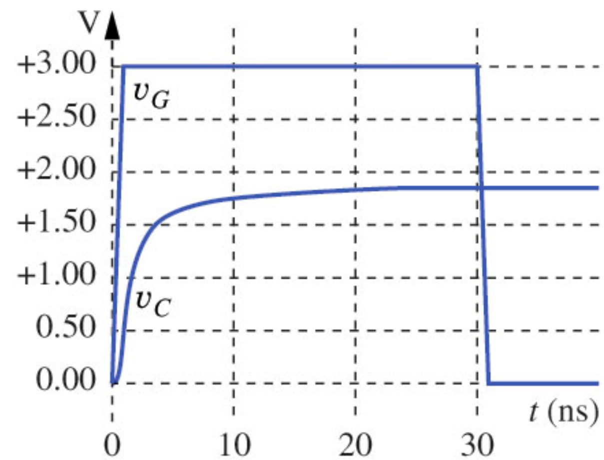
Storing a "0"





(a)

Storing a "1"



The 1-T Cell

Data Storage (cont.)

- Notice that the voltage stored on the storage capacitor on the previous slide does not reach V_{DD}
- It instead is determined by the following:

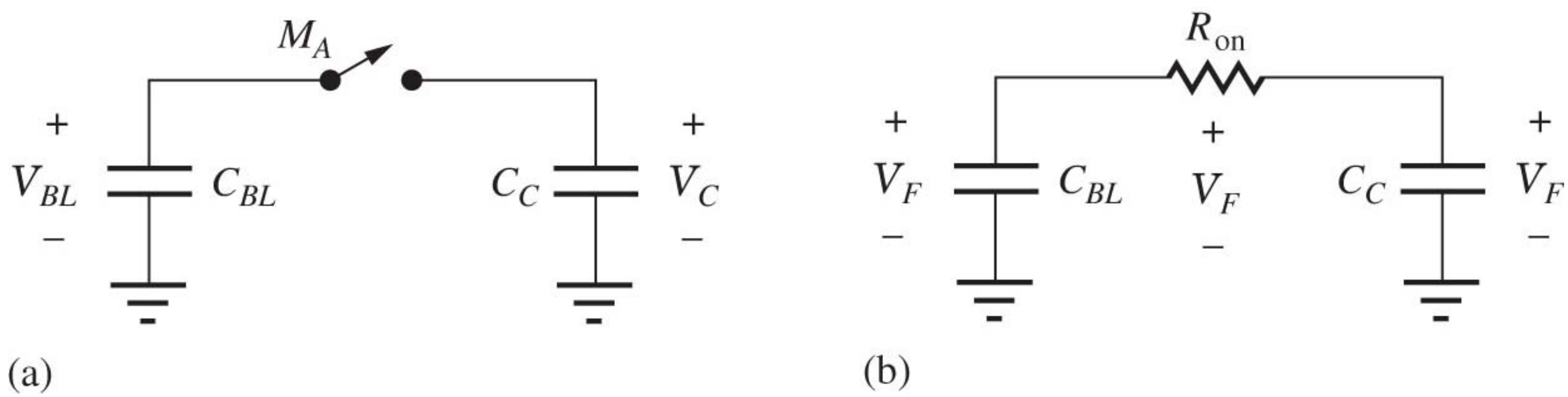
$$V_C = V_G - V_{TN}$$

$$V_C = V_G - \left[V_{TO} + \gamma\left(\sqrt{V_C + 2\phi_F} - \sqrt{2\phi_F}\right)\right]$$

- This is similar to the impact of body effect in the saturated load inverter.

The 1-T Cell
Data Storage (cont.)

- To read a DRAM cell, the bitline is precharged to either V_{DD} or $V_{DD}/2$, and then M_A is turned on



The 1-T Cell

Data Storage (cont.)

- The charge stored on C_C will be shared with C_{BL} through the process of charge sharing, where the read voltage varies slightly

$$V_F = \frac{C_{BL}V_{BL} + C_C V_C}{C_{BL} + C_C} \cong V_{BL}$$

- Normally $C_{BL} >> C_C$, and the charging time constant is: $\tau = R_{ON}\frac{C_{BL}C_C}{C_{BL} + C_C} \cong R_{ON}C_C$